[Attorney list on signature page]

IN THE UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA — SAN JOSE DIVISION

RAMBUS INC., Plaintiff, v. HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA INC., HYNIX SEMICONDUCTOR MANUFACTURING AMERICA INC., SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG AUSTIN SEMICONDUCTOR, L.P., NANYA TECHNOLOGY CORPORATION, NANYA TECHNOLOGY CORPORATION U.S.A., Defendants.	Case No. C 05-00334 RMW **MANUFACTURERS' JOINT MOTION FOR SUMMARY JUDGMENT OF (1) NON-INFRINGEMENT OF THE WARE PATENTS-IN-SUIT UNDER MANUFACTURERS' PROPOSED CLAIM CONSTRUCTION, OR (2) INVALIDITY OF WARE PATENTS-IN-SUIT UNDER RAMBUS'S PROPOSED CLAIM CONSTRUCTION; MEMORANDUM OF POINTS AND AUTHORITIES [FED. R. CIV. P. 56]** **Date: March 26, 2008** **Time: 9:00 a.m.** **Judge: Hon. Ronald M. Whyte** **Courtroom 6, 4th Floor**
RAMBUS INC., Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG AUSTIN SEMICONDUCTOR, L.P., Defendants.	Case No. C 05-02298 RMW
RAMBUS INC., Plaintiff, v. MICRON TECHNOLOGY, INC. and MICRON SEMICONDUCTOR PRODUCTS, INC., Defendants.	Case No. C 06-00244 RMW

TABLE OF CONTENTS

TABLE OF AUTHORITIES

Page

CASES

STATUTES

TABLE OF AUTHORITIES
(continued)

Page

RULES

NOTICE OF MOTION AND MOTION FOR SUMMARY JUDGMENT

Notice is hereby given to Plaintiff Rambus Inc. ("Rambus") and its attorneys of record that on March 26, 2008, or as soon thereafter as this matter may be heard by the Court, Defendants Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., Samsung Austin Semiconductor, L.P., Hynix Semiconductor Inc., Hynix Semiconductor America Inc., Hynix Semiconductor Manufacturing America Inc., Nanya Technology Corporation and Nanya Technology Corporation U.S.A. (collectively, "Manufacturers") will and hereby do move for summary judgment pursuant to Federal Rule of Civil Procedure 56.

Manufacturers seek an order granting them summary judgment of non-infringement of the Ware patents-in-suit under the Manufacturers' proposed claim construction, or, in the alternative, if Rambus's proposed construction is adopted, that the asserted claims of the Ware patents-in-suit are invalid under 35 U.S.C. § 112. This motion is based on this Joint Notice of Motion for Summary Judgment, Memorandum of Points and Authorities, and the pleadings and record in this case.

RELIEF REQUESTED

Pursuant to Rule 56 of the Federal Rules of Civil Procedure, the Manufacturers respectfully seek an Order granting summary judgment of noninfringement in favor of the Manufacturers on Samsung's 2nd Affirmative Defense and Count VIII in its counterclaims; Hynix's 2nd Affirmative Defense and counterclaim 6; Nanya's 2nd Affirmative Defense and counterclaim 5; and Micron's 2nd Affirmative Defense and Counts I-XIV in its counterclaims. Alternatively, if the Court adopts any of Rambus's proposed claim constructions, the Manufacturers seek an Order granting summary judgment of invalidity in favor of the Manufacturers on Samsung's 3rd Affirmative Defense and Count IX in its counterclaims; Hynix's 3rd Affirmative Defense and counterclaim 7; Nanya's 3rd Affirmative Defense and counterclaim 6; and Micron's 4th Affirmative Defense and Counts I-XIV in its counterclaims.

MEMORANDUM OF POINTS AND AUTHORITIES

I. INTRODUCTION

Rambus has accused certain of Manufacturers' products of infringing three claims of U.S. Patent Nos. 6,493,789 and 6,496,897 (collectively "the Ware patents-in-suit").[1] The Accused Products, however, do not include at least two limitations in the asserted claims and, thus, do not infringe the Ware patents-in-suit.[2]

First, the asserted claims are not infringed because the accused products do not meet the "mask bit" limitation. The Manufacturers' proposed construction for this term is "one of eight bits in a write-enable word." None of the Manufacturers' accused products receive an eight-bit write enable word, and thus cannot receive a single bit of this non-existent word. Accordingly, the asserted claims are not infringed.

Second, the asserted claims are not infringed because the Accused Products do not meet the "during a first half of a clock cycle" and "during a second half of a clock cycle" limitations. This is true whether or not the Court adopts the Manufacturers' proposed construction of "mask bit." The Accused Products do not sense the data mask or the data bits during a clock cycle, instead they sense them on the cross point of a differential data strobe signal DQS, /DQS. Moreover, both the data mask signal DM and the incoming bus data DQ in the Accused Products are present over two separate half clock cycles (*i.e.*, they span the first and second half of a clock cycle) and thus are not sensed "during" a specific half clock cycle. Therefore, there is no infringement of the asserted claims.

Finally, if the Court adopts Rambus's proposed claim construction for the "mask bit" limitation, the asserted claims are invalid because the patent specification does not include an adequate written description of "data mask signals." The specification for the Ware patents-in-suit only describes the use of write enable signals in a particular manner in order to control write

[1] The asserted claims are claim 13 of the '798 patent, and claims 2 and 16 of the '897 patent. These are collectively referred to as "the asserted claims."

[2] The Accused Products categories are: gDDR2, DDR2 and DDR3 products for Samsung; DDR2, GDDR3 and RLDRAM for Micron; GDDR3 and DDR2 for Hynix; and DDR2 for Nanya.

operations in a DRAM. There is no description of the data mask signals against which Rambus now asserts infringement.

II. STATEMENT OF FACTS

A. The Ware Patents-In-Suit

The Ware patents-in-suit are directed to DRAMs that receive write enable (WE) information from a DRAM master to control the write operations of the DRAM. The described DRAMs include control logic circuitry that either enables or disables the write operations of the DRAM depending upon the write enable information received by the DRAM. '789 patent at 6:31-49.[3] The write enable information disclosed in the Ware patents-in-suit is made up of write enable (WE) bits, which are received by the DRAM either (1) as an 8-bit write-enable (WE) word, described by the patent as a "mask," or (2) serially in one-bit write-enable signals, which are not described by the Ware patents-in-suit as a "mask." '789 patent at 9:15-16, at 9:23-24. Significantly, the Ware patents-in-suit do not use the term "mask" as that term was commonly used in the art in 1995 (see supra at 19), but rather consistently refer to the 8-bit write-enable (WE) word as a write enable (WE) "mask." This 8-bit write-enable (WE) "mask" is received synchronously with the external clock signal, and each bit of the "mask" masks an individual byte within the data. '789 patent at 9:10-11; 9:45-46; 10:60; 11:40. The 8-bit write enable mask 504 is illustrated in Figure 13A from the '789 patent, which is set forth below.

[3] The '789 and '897 patents have the same specification. As with the Manufacturers' claim construction brief, all references to column and line numbers in the patent specification will be made with reference to the '789 patent.

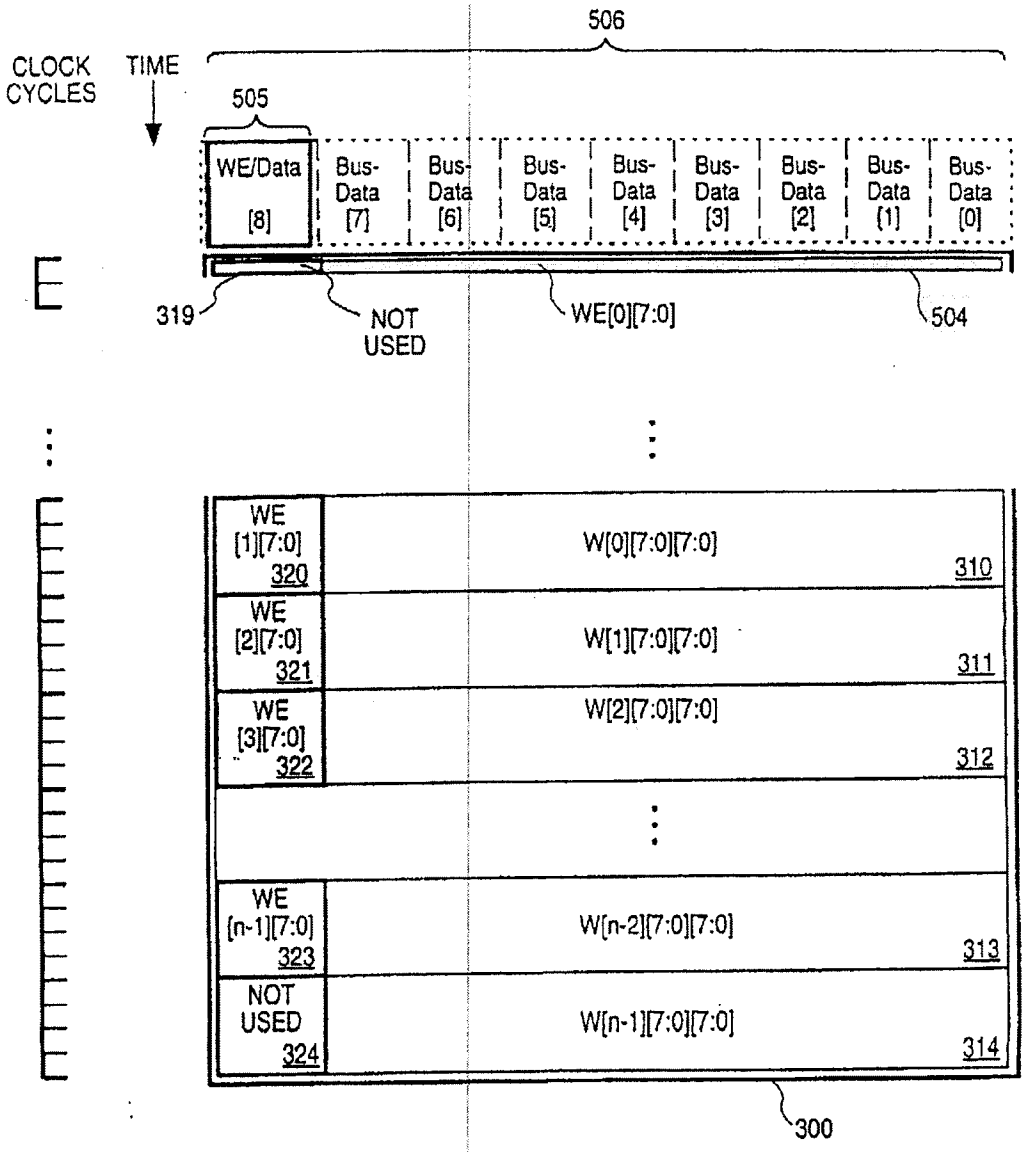

506
CLOCK CYCLES
TIME
505
WE/Data [8]
Bus-Data [7]
Bus-Data [6]
Bus-Data [5]
Bus-Data [4]
Bus-Data [3]
Bus-Data [2]
Bus-Data [1]
Bus-Data [0]
319
NOT USED
WE[0][7:0]
504
WE [1][7:0] 320
W[0][7:0][7:0] 310
WE [2][7:0] 321
W[1][7:0][7:0] 311
WE [3][7:0] 322
W[2][7:0][7:0] 312
WE [n-1][7:0] 323
W[n-2][7:0][7:0] 313
NOT USED 324
W[n-1][7:0][7:0] 314
300

FIG. 13A

As originally filed, the claims of the parent application that ultimately matured into the Ware patents-in-suit did not recite the use of ""mask"" bits. Rather, they recited the use of write enable signals. For example, original claim 1, filed in 1995, provided:

> 1. A method for providing a memory with data and write enable signals, comprising the steps of:
>
> (A) providing the memory with a serial sequence of write enable signals;
>
> (B) providing the memory with data that is offset in time with respect to the serial sequence of write enable signals.

See McAlexander SJ Decl. ¶ 228, Ex. 32 at pg. 33.

The first claims to use the term "mask bit" were filed on June 29, 2000, during the prosecution of application serial no. 09/480,825, which is the ultimate parent of the Ware patents-in-suit. McAlexander SJ Decl. ¶229, Ex. 33 at pp. 1-5 . This addition occurred nearly five years after the original Ware patent application was filed in October 1995.

B. The Accused Products

Rambus has accused DDR2 SDRAM products from each manufacturer of infringing the Ware patents-in-suit.[4] Because the Court is generally familiar with DRAM and its operation, a detailed technical explanation of DRAM and its operation is not included, but is provided in the declaration of Joe McAlexander submitted herewith. McAlexander SJ Decl. ¶¶ 19-33. An explanation of the relevant features of DDR2 SDRAM specific to the Ware patents-in-suit is, however, provided herein.

1. The Representative Accused Nanya Product

Nanya has identified its 512Mb DDR2 SDRAM product, Nanya Part No. NT5TU64M8AE(Green), as being representative of the accused DDR2 SDRAM products

[4] By its Counterclaim in reply, Rambus has asserted that the Manufacturers' DDR3 and GDDR4 products infringe the Ware patents-in-suit. These counterclaims-in-reply are the subject of motions to strike made by Micron, Nanya and Samsung, who contend that DDR3 products should not properly be part of this case. The Manufacturers' respective motions to strike are set for hearing before the Court on October 26, 2007. Should the Court deny these motions, Manufacturers expect to seek leave to supplement their motions for summary judgment to include any newly added products.

manufactured by Nanya (hereinafter the "Nanya Representative Product").[5] The Nanya representative product is a JEDEC-compliant DDR2 SDRAM product. McAlexander SJ Decl. ¶ 206, Ex. 24 at NTCR-00054416, 00054423. Because the asserted claims of the Ware patents-in-suit involve write operations, the technical discussion of Nanya's representative part will focus on how it performs write operations.

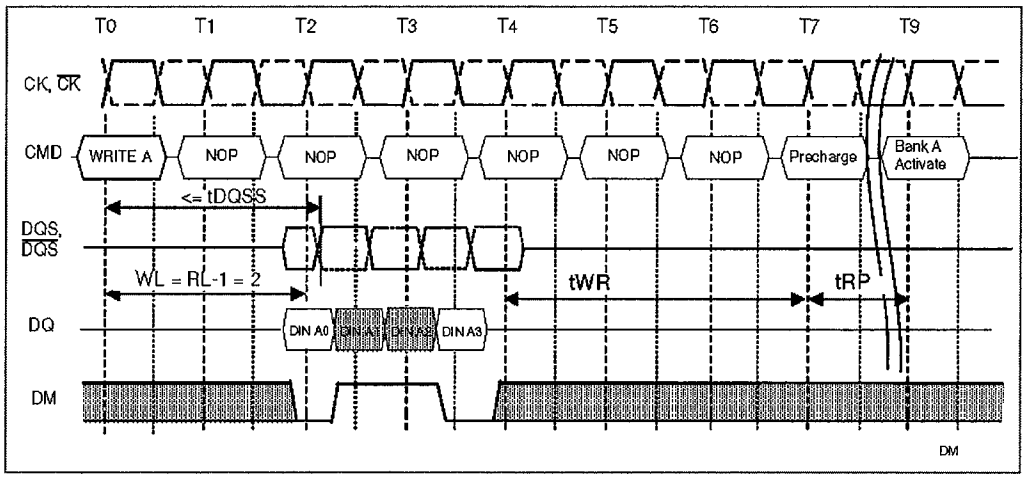
During operation, the Nanya representative product receives a differential external clock CK, /CK and various incoming address and control signals from an external memory controller. McAlexander SJ Decl. ¶ 207, Ex. 24 at NTCR-00054420, 00054423, 00054436, 00054437. The Nanya representative product responds to the incoming address and control signals and performs operations based on those commands. During the process of receiving commands, the address and control signals are sensed by the DRAM at a specific point in time – once per clock cycle at the crossing point of the rising edge of the clock signal CK and the falling edge of the complementary clock signal /CK. McAlexander SJ Decl. ¶ 208, Ex. 24 at NTCR-00054420, 00054444. During write operations, which are the focus of the Ware patents-in-suit, the Nanya representative product receives data to be written to the memory array. McAlexander SJ Decl. ¶¶ 209-211. The data is supplied from the bus on data signal lines DQ0-DQ7. McAlexander SJ Decl. ¶ 212, Ex. 24 at NTCR-00054417 [Pin diagram]. The DRAM senses the bus data DQ at a time point that is specified by a differential data strobe signal, which is identified in the timing diagrams as DQS, /DQS. McAlexander SJ Decl. ¶ 211, Ex. 24 at NTCR-00054420, 00054437.

The Nanya representative product initiates a memory operation upon receiving a command that comprises a combination of the following control signals: /CS, /RAS, /CAS, and /WE, wherein each combination of control signals has a predefined meaning. McAlexander SJ Decl. ¶ 208, Ex. 24 at NTCR-00054420, 00054436, 00054437. One of these control signals is a write enable signal /WE. McAlexander SJ Decl. ¶ 209, Ex. 24 at NTCR-00054420, 00054436, 00054437. The DRAM performs a write operation when the following signals are sensed by the DRAM: /CS low; /RAS high; /CAS low; /WE low. McAlexander SJ Decl. ¶210, Ex. 24 at

[5] Similar representative products have been identified by Hynix, Samsung and Micron.

NTCR00054467. The timing of a burst write operation is illustrated in the timing diagram below. McAlexander SJ Decl. ¶ 210, Ex. 24 at NTCR-00054444.

Burst Write Operation with Data Mask : RL = 3 (AL = 0, CL = 3), WL = 2, tWR = 3 , BL = 4



As shown in this figure and explained above, in the line labeled CMD and the item labeled "Write A," the Nanya representative product senses the control signals once per external clock cycle on the crossing of the rising edge of the clock signal CK and falling edge of the complementary clock signal /CK. McAlexander SJ Decl. ¶ 207, Ex. 24 at NTCR-00054420, 00054444, 00054447. At a specified point in time after sampling the write command, the Nanya representative product senses the incoming bus data, shown in the Figure on the line labeled DQ as DIN A0, DIN A1, DIN A2 and DIN A3. McAlexander SJ Decl. ¶ 211. The incoming data is sensed by the Nanya representative product at a crossing point of the differential data strobe signal, shown in the line labeled DQS, /DQS in the figure. McAlexander SJ Decl. ¶ 208, Ex. 24 at NTCR-00054420, 00054426-00054429, 00054444, 00054447.

As shown above, the Nanya representative product senses the data received from the bus. McAlexander SJ Decl. ¶ 212, Ex. 24 at NTCR-00054416. The designator DIN A0, etc. shown in the above figure represents 8 bits (one byte) of data received by the Nanya representative product. McAlexander SJ Decl. ¶ 212. The data mask signal, shown in the figure on line DM,

accompanies the received data and can mask (or block) a particular byte of incoming bus data so that none of the eight incoming data bits are written to the memory array, depending on whether the signal DM is high or low. McAlexander SJ Decl. ¶ 213, Ex. 24 at NTCR-00054420, 00054447. A particular data byte is written to the memory array only if the data mask signal DM is low. McAlexander SJ Decl. ¶ 213, Ex. 24 at NTCR-00054420, 00054447. This is exemplified in the figure for data DIN A0 and DIN A3, where the data mask signal DM is low. When the data mask signal DM is high, the Nanya representative product ignores the incoming data. McAlexander SJ Decl. ¶ 213, Ex. 24 at NTCR-00054447. This is exemplified in the above figure for data DIN A1 and DIN A2, where the data mask signal is high, and the data is not written to the array. Data masks such as the masks used in the DDR2 SDRAM can be used to prevent over-writing data that is already stored in the array, and are particularly useful in graphics applications where only some of the sections of a picture change. McAlexander SJ Decl. ¶ 214.

2. The Representative Hynix, Samsung, and Micron Products

Hynix, Samsung, and Micron each have also identified representative DDR2 products. The representative Hynix, Samsung, and Micron DDR2 products operate in the same manner that as that of the Nanya representative product discussed above with respect to the features and functionality at issue in this motion.

The representative Hynix products are Hynix Part Nos. HY5PS12421FP, HY5PS12821FP, and HY5PS121621FP and are configured for use with four-bit, eight-bit, and sixteen-bit bus data, respectively. Each Hynix product is a JEDEC-compliant 512Mb DDR2 SDRAM product with four memory arrays (or banks) and can interface with an external computer bus. McAlexander SJ Decl. ¶ 191. The four- and eight-bit representative Hynix products operate in the same manner that as that of the Nanya representative product discussed above with respect to the use of data masks and write enable signals for purposes of this motion. The sixteen-bit representative Hynix product receives one write enable signal /WE and senses two data mask signals during write operations: an upper data mask UDM for masking the upper byte (8 bits) of

the incoming data and a lower data mask LDM for masking the lower byte (8 bits) of the incoming bus data. McAlexander SJ Decl. ¶¶ 191 - 198.

The representative Samsung DDR2 (and gDDR2) product is a JEDEC-compliant 1Gb DDR2 SDRAM product, Samsung Part No. K4T1G084QA, that has eight memory arrays (or banks) and can interface with an external computer bus. McAlexander SJ Decl. ¶ 157. The representative Samsung product supports eight-bit bus data and operates in the same manner that as that of the Nanya representative product discussed above in Section II.B.1 with respect to the use of data masks and write enable signals for purposes of this motion. McAlexander SJ Decl. ¶¶ 157 - 163. The representative Samsung GDDR3 product is a GDDR3 SDRAM product, which operates in a similar manner as that of the Nanya representative product discussed above in Section II.B.1 with respect to the features and functionality at issue in this motion. McAlexander SJ Decl. ¶¶ 164 - 170.

The representative Micron DDR2 products are JEDEC-complaint 256Mb and 512Mb DDR2 SDRAM products, which have four memory arrays (or banks) and can interface with an external computer bus. McAlexander SJ Decl. ¶ 171. These representative Micron DDR2 products are configured for use with sixteen-bit bus data and operate in the same manner that as that of the sixteen-bit representative Hynix product discussed above with respect to the use of data masks and write enable signals for purposes of this motion. McAlexander SJ Decl. ¶¶ 171 - 177. The other representative Micron products are a GDDR3 SDRAM product and a 288 Mb CIO Reduced Latency DRAM product (RLDRAMII), which operate in a similar manner as that of the representative Nanya product discussed above with respect to the features and functionality at issue in this motion.

III. SUMMARY JUDGMENT OF NON-INFRINGEMENT

As demonstrated herein and in the accompanying declaration of Joseph McAlexander, adoption of the Manufacturers' proposed claim constructions for the "mask bit" term or the "during a first/second half of a clock cycle of an external clock signal" will render summary judgment of noninfringement appropriate.

B. Manufacturers' Accused Products Do Not Infringe The Accused Claims Under The Manufacturers' Proposed Claim Construction

1. The Manufacturers' Accused Products Do Not Have The 8-Bit Write Enable Masks Required By The Asserted Claims

The Manufacturers' proposed construction of "mask bit" is: "one of eight bits in a write-enable word." Joint Claim Construction Statement ("JCCS"), App. A at 49. This term is found in all asserted claims from the Ware patents-in-suit. The accused products do not receive an "eight bit write enable word" and, thus, cannot use a single bit of such a word in the manner required by the claims. McAlexander SJ Decl. ¶ 215.

In its Preliminary Infringement Contentions required by the Patent Local Rules, Rambus alleged that the data mask DM is the "mask bit" of the claims. McAlexander SJ Decl. Ex. 30 at 23, 25, 27-28. The identified data mask DM does not meet the "mask bit" claim limitation as properly construed. McAlexander SJ Decl. ¶ 217. Rambus no doubt hopes to confuse the trier of fact with the use of the term "mask". The data mask signal DM received by the accused products (as described above in Section II.B) is not the "mask" defined by the patent. Rather, it is the data mask that was commonly understood and used in the art in 1994, and which is very different than the "mask" of the Ware patent.

To begin, the Ware "mask" is an eight-bit word and is received synchronously with the external clock signal. In contrast, the data mask DM received by the Accused Products is a separate, individual signal and is received synchronously with the data strobe signal DQS, /DQS (or write data strobe signals WDQS0-3 in GDDR3 accused products or input data clock signals DK, DK# in RLDRAM accused products). McAlexander SJ Decl. ¶ 216. In the Nanya representative product, for example, which senses eight bits of data at a time, the entire byte of incoming bus data will not be written to the memory array if the data mask signal DM is high. McAlexander SJ Decl. ¶ 218. In DDR2 SDRAM products, such as the Micron DDR2 representative products, that sense a sixteen-bit data bus, two data mask signals are used: an upper data mask UDM for masking the upper byte (8 bits) of the incoming data and a lower data mask LDM for masking the lower byte (8 bits) of the incoming bus data. McAlexander SJ Decl. ¶ 216. In GDDR3 SDRAM products, such as the Micron GDDR3 representative product, that sense a

A. Legal Framework for Summary Judgment of Noninfringement

Literal infringement requires that "every limitation recited in the claim appear[ ] in the accused product, i.e., when the properly construed claim reads on the accused device exactly." *DeMarini Sports, Inc. v. Worth, Inc.*, 239 F.3d 1314, 1331 (Fed. Cir. 2001) (citation omitted). Infringement under the doctrine of equivalents requires there to be "insubstantial" differences between the accused products and the claim limitations or for the accused products to satisfy the "function, way, result" test. *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd.*, 493 F.3d 1368, 1377 (Fed. Cir. July 5, 2007) (citing *Graver Tank & Manufacturing Co. v. Linde Air Products Co.*, 339 U.S. 605 (1950)).

Rambus bears the burden of proving infringement. *Exigent Tech., Inc. v. Atrana Solutions, Inc.*, 442 F.3d 1301, 1309-10 (Fed. Cir. 2006). As a result, the Manufacturers are not required to produce evidence showing the lack of a genuine issue of material fact. *Celotex Corp. v. Catrett*, 477 U.S. 317, 325 (1986). Rather, the Manufacturers only need to show "an absence of evidence to support the nonmoving party's case." *Id.* at 325. Rambus, as the nonmoving party, must "come forward with 'specific facts showing that there is a genuine issue for trial'" in order to successfully oppose this motion. *Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 475 U.S. 574, 587 (1986) (*quoting* Fed. R. Civ. P. 56(e)).

Summary judgment is "designed to secure the just, speedy and inexpensive determination of every action." *Celotex Corp. v. Catrett*, 477 U.S. 317, 327 (1986) (internal quotations omitted). The Manufacturers seek summary judgment of noninfringement based on each of the following three independent grounds: (1) there is no factual dispute that the Accused Products do not meet the "mask bit" limitation, which should be construed to require the use of an eight-bit write enable word; and (2) there is no factual dispute that the Accused Products do not meet the "during a first/second half of a clock cycle of an external clock cycle" limitations.[6]

[6] While there are no factual disputes regarding the structure and operation of the Accused Products relevant to the issues presented in this motion, there may be factual disputes regarding the Accused Products with respect to other issues that may arise in this litigation, including factual issues with respect to these claim limitations if the Court adopts Rambus's proposed constructions.

thirty-two bit data bus, four data mask signals are used: DM0-3, each masking a set of 8 bits of the 32 incoming bus data. McAlexander SJ Dec. ¶ 219. In Micron RLDRAM II products that sense a thirty-six bit data bus, a DM signal is used for masking all 36 bits of the incoming bus data.

The Accused Products each receive, and respond to, the data mask signal DM, UDM, LDM and DM0-3 in the same manner, for purposes of this motion, as the Nanya and Micron DDR2 products.[7] McAlexander SJ Decl. ¶ 215. These data mask signals are not part of an 8-bit write enable word, and thus do not satisfy the properly construed claim limitation.

Further, as described above, the data mask signals of the Accused Products are substantially different than the 8-bit write enable "mask" of the Ware patents-in-suit and thus the data mask signals of the Accused Products are not equivalent to the "mask bit" of the patent.

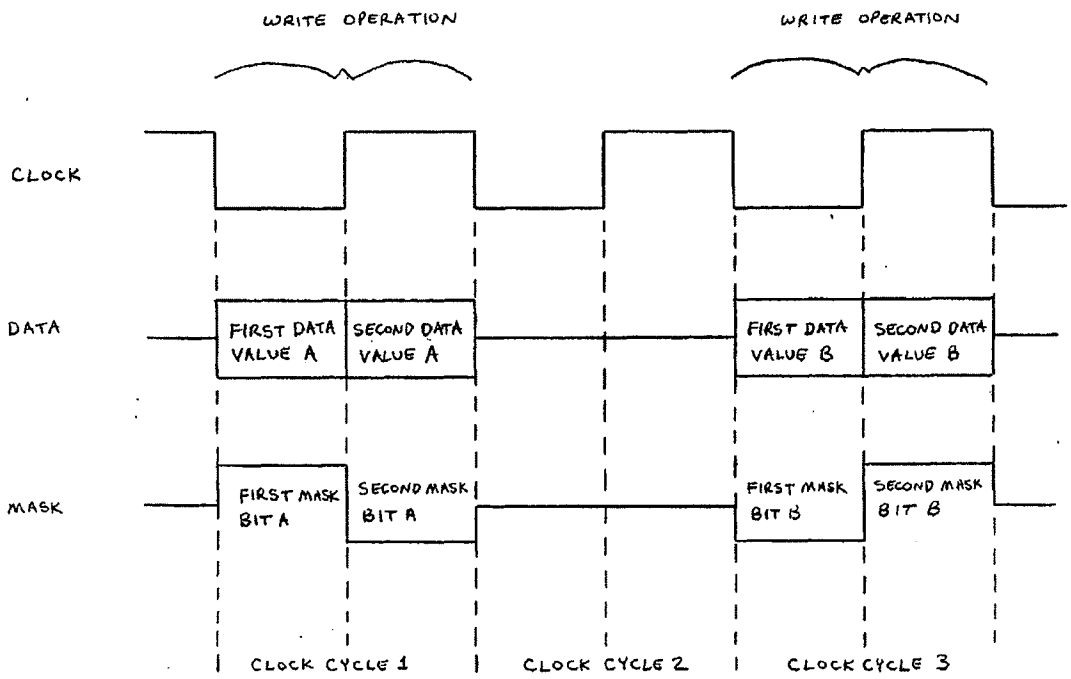
2. The Accused Products Do Not Receive Data Masks or Data Bits During A Half Clock Cycle Of An External Clock Signal

As an initial matter, the Court only needs to consider this claim limitation if it adopts Rambus's definition of the term "mask bit." If the Court does so, however, all asserted claims are still not infringed because the mask bit is not received "during a first half of a clock cycle of an external clock signal" or "during a second half of a clock cycle of an external clock signal" as required by all asserted claims. '789 Patent, claim 8 (at 14:52-59); '897 Patent, claims 1 and 13 (at 13:58-65; at 14: 40-44). The Manufacturers' proposed construction of "during a first/second half of a clock cycle of an external clock signal" is: "only between two adjacent clock edges beginning with a rising edge of the clock signal and ending at the following falling edge" or "only between two adjacent clock edges beginning with a falling edge of the clock signal and ending at the following rising edge." JCCS App. A at 49.

To assist the Court in understanding the Manufacturers' arguments, the Manufacturers' have prepared a representative timing diagram that illustrates the data/mask bit relationship

[7] The accused GDDR3 products do not use a differential strobe, but instead use a single write strobe signal. Also, the GDDR3 products have 32 data lines that are divided into 4 sets of 8 data lines. The GDDR3 parts also use 4 data mask signals DM0-3, each corresponding to a set of 8 data lines and a write data strobe signal.

required by the asserted claims – namely that the mask bit and the data bit be received exactly within the boundaries of a half clock cycle of the external clock. McAlexander SJ Decl. ¶ 220. In this diagram, two write operations are performed during CLOCK CYCLE 1 and CLOCK CYCLE 3, respectively – each write operation taking place during half of its respective clock cycle. McAlexander SJ Decl. ¶ 221.

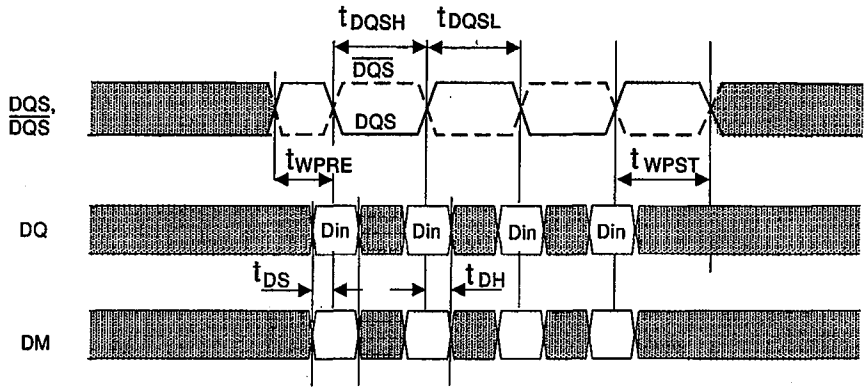


As shown above, both FIRST DATA VALUE A and FIRST MASK BIT A are received "during a first half" of CLOCK CYCLE 1 because they are entirely between the two clock edges of the half cycle. McAlexander SJ Decl. ¶ 221. Similarly, both SECOND DATA VALUE A and SECOND MASK BIT A are received "during a second half" of CLOCK CYCLE 1 for the same reason. McAlexander SJ Decl. ¶ 221.[8] Similarly, both SECOND DATA VALUE A and SECOND MASK BIT A are received "during a second half" of CLOCK CYCLE 1 for the same

[8] Similarly, FIRST DATA VALUE B and FIRST MASK BIT B each are shown as being received "during a first half" of CLOCK CYCLE 3, and SECOND DATA VALUE B and SECOND MASK BIT B each are received "during a second half" of CLOCK CYCLE 3. McAlexander SJ Decl. ¶ 222.

reason. McAlexander SJ Decl. ¶ 221. In each instance, the relevant data value and mask bit both are received during the same half clock cycle, and neither the data value nor the mask bit extend beyond the designated half clock cycle. McAlexander SJ Decl. ¶¶ 221, 222.

As explained above, Rambus has asserted that the Accused Products meet this claim limitation by virtue of their use of the data mask signal DM. McAlexander SJ Decl. Ex. 30 at 23, 25, 27-28. Comparing the demonstrative timing diagram set forth above with the timing diagram of Nanya's Representative Product shows that the Accused Products clearly do not meet the first/second clock cycle limitations. In the Nanya Representative Product, the data mask signal DM is sensed synchronously with the differential data strobe signal DQS, /DQS at the same time as the incoming bus data is sensed. McAlexander SJ Decl. ¶ 223.



McAlexander SJ Decl. ¶ 223; Ex. 24 at NTCR-00054447. Comparing the above figure with the demonstrative figure showing the timing arrangement required by the claims illustrates why this claim limitation is not met. The Accused Products sense the incoming bus data (shown in the figure as DQ) and the data mask signal (shown in the figure as DM) synchronously with the crossing edges of the differential data strobe signal DQS, /DQS (or the edges of the write data strobe signals WDQS0-3 for the GDDR3 SDRAM accused products or the differential input data clock signals DK, DK# for the Micron RLDRAM II accused products). McAlexander SJ Decl. ¶ 224. The asserted claims, in contrast, require the data to be sensed synchronously with respect

to the external clock signal – a signal that is different from the differential data strobe DQS, /DQS (or write data strobe signals WDQS0-3 for the GDDR3 SDRAM accused products or the differential clock DK, DK# for the Micron RLDRAM II accused products). McAlexander SJ Decl. ¶ 226. In addition, the data mask signal DM of Fig. 12 spans more than one clock cycle; in other words, it is not received "during" a half clock cycle, but is rather present on the pins over portions of two different half clock cycles. The data mask signal DM in the accused DDR2 and RLDRAM products and the data mask signals DM0-3 in the GDDR3 products also span more than one-half clock cycle. In contrast, the claimed first and second mask bits required by the Ware patents-in-suit must be present during a designated half clock cycle as shown in the demonstrative figure. McAlexander SJ Decl. ¶ 226. Accordingly, these claim limitations are not met by the data mask DM, UDM, and LDM.

For the reasons set forth above, the timing of the data mask DM in the Accused Products is substantially different than the timing required by the claims, and is not equivalent thereto.

IV. SUMMARY JUDGMENT OF INVALIDITY

As demonstrated herein and in the accompanying declaration of Joseph McAlexander, adoption of Rambus's proposed claim constructions for the "mask bit" term renders summary judgment of invalidity appropriate under 35 U.S.C. § 112.

A. The Claims Are Invalid For Lack Of Written Description Under § 112, ¶ 1

1. Legal Framework for Summary Judgment of Invalidity

Compliance with the statutory written description requirement, set forth in 35 U.S.C. § 112, ¶ 1, is essential for the validity of a patent. The purpose of the written description requirement is to "ensure that the scope of the right to exclude, as set forth in the claims, does not overreach the scope of the inventor's contribution to the field of art as described in the patent specification." *Univ. of Rochester v. G.D. Searle & Co., Inc.*, 358 F.3d 916, 920 (Fed. Cir. 2004) *citing Reiffin v. Microsoft Corp.*, 214 F.3d 1342, 1345 (Fed. Cir. 2000)).

The written description requirement is premised on the fundamental notion that patents must provide notice to the public, in the initial application, consistent with the scope of the

claims. To fulfill the written description requirement, the patent specification "must describe the invention sufficiently to convey to a person of skill in the art that the patentee had possession of the claimed invention at the time of the application, i.e., that the patentee invented what is claimed." *LizardTech, Inc. v. Earth Resource Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed. Cir. 2005). An applicant complies with the written description requirement by "such descriptive means as words, structures, figures, diagrams, formulas, etc., that fully set forth the claimed invention." *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997) A narrow disclosure will limit claim breadth, because the scope of a claim cannot be "greater than what a person of skill in the art would understand the inventor to possess." *LizardTech*, 424 F.3d at 1346. The mandates of public notice do not allow any gaps between claim scope and the patent's disclosure to be satisfied by what those skilled in the art may consider to be "an obvious variant of that which is disclosed in the specification." *Lockwood*, 107 F.3d at 1572. "It is not sufficient for the purposes of the written description requirement of § 112 that the disclosure, when combined with the knowledge in the art, would lead one to speculate as to modifications that the inventor might have envisioned, but failed to disclose." *Id.*

Because the written description must provide notice of the boundaries of the claims, a patent's disclosure of a species does not necessarily provide sufficient written description support for a claim more broadly directed to the genus. The Federal Circuit emphasized this point in *Bilstad v. Wakalopulos*, 386 F.3d 1116, 1124-25 (Fed. Cir. 2004), where it provided two examples of disclosure of a species that would not support a genus claim. Although the court gave as one example "unpredictability in the particular field" (*id.* at 1125), *Bilstad* did not establish that "unpredictability in the art" is necessary for a finding of lack of enablement. Rather, *Bilstad* provided a second example where disclosure of a species would not support a genus claim: where the specification distinguishes the prior art as inferior and touts the advantage of a certain species. Id. In so doing, the court relied on *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1158 (Fed. Cir. 1998):

> Another exception [to disclosure of a species supporting a genus claim] is presented in *Tronzo* .... In *Tronzo*, this court held that substantial evidence did not

> support the jury's verdict that claims to a hip prosthesis of generic shape were supported by a parent disclosing only a trapezoidal shape. We said, "Instead of suggesting that the 589 patent [the parent] encompasses additional shapes, the specification specifically distinguishes the prior art as inferior and touts the advantages of the conical shape of the 589 cup. Such statements make clear that the 589 patent discloses only conical shaped cups and nothing broader."

Id.

The Federal Circuit has not hesitated to uphold summary adjudications of invalidity of patents that fail to adhere to the written description requirement. *See, e.g.*, *LizardTech*, 424 F.3d at 1346-47 (affirming grant of summary judgment of invalidity where patent specification's description of a particular method for creating a seamless discrete wavelet transform ("DWT") for digital image compression was insufficient as a matter of law to support disputed claim that broadly covered other methods of seamless DWT). In affirming the grant of summary judgment in *LizardTech*, the Federal Circuit also built upon the analysis of its earlier holding in *Tronzo*, which recognized that claims in a later-filed application are not entitled to the filing date of an earlier application under 35 U.S.C. § 120, unless the earlier application complies with the written description requirement. The *Tronzo* court held that, to meet the written description requirement, "the disclosure of the earlier application, the parent, must reasonably convey to one of skill in the art that the inventor possessed the later-claimed subject matter at the time the parent application was filed." *Id.* (emphasis added). *LizardTech* confirms that, although cases such as *Tronzo* dealt specifically with the issue of whether a patent was entitled to claim priority to a prior application, the test for satisfaction of the written description requirement is identical where, as here, the issue is whether claims issued in continuation applications are described in the parent specification. *See also Rochester*, 358 F.3d at 924 ("[T]he basic requirement of a written description of an invention exists whether a question of priority has arisen or not. The statute does not limit the requirement to cases in which a priority question arises.").

Thus, although compliance with the written description requirement is a question of fact, summary judgment is appropriate in cases such as this, where it is beyond dispute that the narrow description in the patent specification cannot support claims of broader scope. *See LizardTech*, 424 F.3d at 1346; *Rochester*, 358 F.3d at 927 (noting that "a patent can be held invalid for failure

to comply with the written description requirement, based solely on the language of the patent specification"). "After all, it is in the patent specification where the written description requirement must be met." *Rochester*, 358 F.3d at 927.

2. Under Rambus's Construction — The Ware patents-in-suit Lack An Adequate Written Description Of The Claimed Mask Bit

Rambus's proposed construction of "mask bit" is a "binary digit indicating whether to write data." This construction improperly broadens the scope of the asserted claims beyond what Rambus described in the Ware patent specification. Rambus now argues that this term is sufficiently broad to encompass data mask signals (DM, UDM, LDM and DM0-3) used in modern DRAM products. McAlexander SJ Decl. Ex. 30 at 23, 25, 27-28.

There is no written description of such a signal in the Ware patent specification, nor is the term "mask bit" used in the Ware specification. Instead, the Ware disclosure is limited to control of a DRAM using write enable signals received by the memory in either one-bit write-enable signals or eight-bit write-enable words, the latter being referred to as "masks." '789 Patent, At 9:8-12. The Ware patent specification consistently uses the term "mask" only to describe an eight-bit write-enable word. '789 Patent at 9:8-12; 19-24; 40-47; 10:60-63. Therefore, the original written disclosure only provides written support for a "mask bit" that is one bit within an eight-bit write-enable word, nothing more. There is no disclosure of a data mask signal as used in modern DRAM products. McAlexander SJ Decl. ¶231.

The term "mask bit" also did not appear in the original claims filed in 1995. These claims instead recited the use of serial write enable signals. McAlexander SJ Decl. ¶ 228 Ex. 32 at pg. 33. The first claims containing the term "mask bit" were added on June 29, 2000, nearly five years after the first Ware application was filed, presumably in an attempt to expand the scope of the patent to try and capture modern DRAM products. McAlexander SJ Decl. ¶ 3 Ex 33 at pp. 1-5. The later addition of this claimed feature supports the conclusion that the claims do not meet the written description requirement. *See, e.g.*, *PIN/NIP, Inc. v. Platte Chem. Co.*, 304 F.3d 1235, 1247-48 (Fed. Cir. 2002) (finding added claim invalid for lack of written description); *see also*

Chiron Corp. v. Genentech, Inc., 363 F.3d 1247, 1255 (Fed. Cir. 2004) ("The written description requirement prevents applicants from using the amendment process to update their disclosures (claims or specifications) during their pendency before the patent office.").

In 1995, when the original Ware application was filed, data masks were well known, and were known to be separate and distinct signals from write enable signals. McAlexander SJ Decl. ¶ 7. This distinction is evident from JEDEC documents that were published before the filing of the Ware patents-in-suit and that identified write enable signals and data mask signals as separate signals. McAlexander SJ Decl. ¶ 8, Ex. 36 at NTCR-00037145. That these signals were different is confirmed by the fact that these two signals were assigned separate pins in these early products. McAlexander SJ Decl. ¶ 9, Ex. 36 at NTCR-00037132, Ex. 31 at NTCR-00038110, 00038111.

In 1995, a write enable signal /WE was understood to be a control signal that when true caused the incoming bus data DQ to be written into the memory and was received internally in the memory by control logic. McAlexander SJ Decl. ¶ 10. This is consistent with the way that the Ware patents-in-suit describe their write enable signals as enabling or disabling the write operation of the memory and being received internally in the memory by control logic. '789 patent, at 6:31-49. In contrast, a mask data signal was understood to be a separate signal received by the memory to mask (or block) incoming data bytes during a write operation. McAlexander SJ Decl. ¶ 11, Ex. 36 at NTCR-00037145. Because the Ware patent specification uses the term "write enable" and the notation "/WE" consistent with the understanding of write enable signals in the art, one skilled in the would not have recognized Ware's write enable signals, much less the write-enable words, to describe data mask signals.

Given the complete lack of disclosure of data mask signals in the original Ware application, despite the fact that data mask signals were well-known at the time of the original filing, one skilled in the art would not have recognized that the Ware inventors possessed the idea of using data mask signals, or considered that to be part of their invention. Therefore, under Rambus's proposed construction of the term "mask bit," the claims are invalid for failure to comply with the written description requirement.

B. The Claims Are Invalid Under § 112, ¶ 2, For Failure To Claim The Subject Matter Which The Inventors Regarded As Their Invention

If the claims are construed as Rambus requests, they are invalid under 35 U.S.C. § 112, ¶ 2, which provides that: "[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." 35 U.S.C. § 112, ¶ 2 (emphasis added). The Federal Circuit has held that "[w]here it would be apparent to one of skill in the art, based on the specification, that the invention set forth in a claim is not what the patentee regarded as his invention, [the court] must hold that claim invalid under § 112, paragraph 2." *Allen En'g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1349 (Fed. Cir. 2002). While this requirement is related to the written description requirement of § 112, ¶ 1, the determination under § 112, ¶ 2, "like a determination whether a claim is sufficiently definite, 'is a legal conclusion that is drawn from the court's performance of its duty as the construer of patent claims.' Thus, as with claim construction, a determination under either portion of Section 112, second paragraph, is a question of law . . .." *Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 1377 (Fed. Cir. 2000) (quoting *Personalized Media Communications, LLC v. Int'l Trade Comm'n*, 161 F.3d 696, 705 (Fed. Cir. 1998) (citations omitted)).

The above analysis of the Ware specification proves that the subject matter which the applicants regarded as their invention was limited to a device that uses serial write enable signals, or a device that uses eight-bit write enable masks. The specification proves that the inventors did not consider generic data mask signals, known in the art at that time, to be within the subject matter of what they purportedly invented. Rambus's proposed constructions would, however, encompass such subject matter and would render the claims invalid under § 112, ¶ 2. *Allen Eng'g.*, 299 F.3d at 1349.

Regardless of how the Court decides the written description defense under § 112, ¶ 1, the Court must decide the defense under § 112, ¶ 2 as a matter of law. *Solomon*, 216 F.3d at 1377. If the Court adopts Rambus's constructions, the Court should grant the Manufacturers summary judgment of invalidity on this defense.

V. CONCLUSION

For the reasons set forth herein, if the Court adopts the Manufacturers' proposed constructions of the disputed Ware claim terms discussed herein, then the Manufacturers should be found not to infringe the asserted Ware claims. If, on the other hand, the Court adopts Rambus's proposed construction for the term "mask bit", the Court should grant Manufacturers' motion that the asserted claims are invalid for failure to comply with the requirements of 35 U.S.C. § 112.

Dated: October 5, 2007

WEIL, GOTSHAL & MANGES, LLP

By: */s/ David J. Healey*
David J. Healey

MATTHEW D. POWERS (Bar No. 104795)
Email: matthew.powers@weil.com
EDWARD R. REINES (Bar No. 135930)
Email: edward.reines@weil.com
WEIL, GOTSHAL & MANGES LLP
201 Redwood Shores Parkway
Redwood Shores, CA 94065
Telephone: (650) 802-3000
Facsimile: (650) 802-3100

DAVID J. HEALEY (*admitted pro hac vice*)
Email: david.healey@weil.com
ANITA E. KADALA (*admitted pro hac vice*)
Email: anita.kadala@weil.com
WEIL, GOTSHAL & MANGES LLP
700 Louisiana, Suite 1600
Houston, TX 77002
Telephone: (713) 546-5000
Facsimile: (713) 224-9511

Attorneys for Defendants
SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA, INC.,
SAMSUNG SEMICONDUCTOR, INC., and
SAMSUNG AUSTIN SEMICONDUCTOR, L.P.

Dated: October 5, 2007

TOWNSEND AND TOWNSEND AND CREW LLP

By: */s/ Theodore G. Brown III*
Theodore G. Brown III

DANIEL J. FURNISS (Bar No. 73531)
Email: *djfurniss@townsend.com*
THEODORE G. BROWN III (Bar No. 114672)
Email: *tgbrown@townsendf.com*
JORDAN TRENT JONES (Bar No. 166600)
Email: *jtjones@townsendf.com*
TOWNSEND AND TOWNSEND AND CREW LLP
379 Lytton Avenue
Palo Alto, CA 94301
Telephone: (650) 326-2400
Facsimile: (650) 326-2422

KENNETH L. NISSLY (Bar No. 77589)
Email: *kennissly@thelen.com*
SUSAN van KEULEN (Bar No. 136060)
Email: *svankeulen@thelen.com*
GEOFFREY H. YOST (Bar No. 159687)
Email: *gyost@thelen.com*
THELEN REID BROWN RAYSMAN & STEINER LLP
225 West Santa Clara Street, Suite 1200
San Jose, CA 95113
Telephone: (408) 292-5800
Facsimile: (408) 287-8040

KENNETH R. O'ROURKE (Bar No. 120144)
Email: *korourke@omm.com*
WALLACE A. ALLAN (Bar No. 102054)
Email: *tallan@omm.com*
O'MELVENY & MYERS LLP
400 South Hope Street, Suite 1060
Los Angeles, CA 90071-2899
Telephone: (213) 430-6000
Facsimile: (213) 430-6407

Attorneys for Defendants
HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA INC., and HYNIX SEMICONDUCTOR MANUFACTURING AMERICA INC.

WEIL GOTSHAL & MANGES LLP

By: */s/ Jared Bobrow*
Jared Bobrow

JARED BOBROW (BAR NO. 133712)
Email: *jared.bobrow@weil.com*
WEIL GOTSHAL & MANGES LLP
201 Redwood Shores Parkway
Redwood Shores, CA 94065
Telephone: (650) 802-3034
Facsimile: (650) 802-3100

WILLIAM C. PRICE (BAR NO. 108542)
Email: *william.price@quinnemanuel.com*
HAROLD A. BARZA (BAR NO. 80888)
Email: *halbarza@quinnemanuel.com*
JON R. STEIGER (BAR NO. 229814)
Email: *jonsteiger@quinnemanuel.com*
ROBERT J. BECHER (BAR NO. 193431)
Email: *robertbecher@quinnemanuel.com*
QUINN EMANUEL URQUHART OLIVER & HEDGES, LLP
865 South Figueroa Street, 10th Floor
Los Angeles, CA 90017
Telephone: (213) 443-3000
Facsimile: (213) 443-3100

Attorneys For Defendants
MICRON TECHNOLOGY, INC. AND MICRON SEMICONDUCTOR PRODUCTS, INC.

Dated: October 5, 2007

ORRICK HERRINGTON & SUTCLIFFE LLP

By: */s/ Craig R. Kaufman*
Craig R. Kaufman

ROBERT E. FREITAS (Bar No. 80948)
Email: *rfreitas@orrick.com*
CRAIG R. KAUFMAN (Bar No. 159458)
Email: *ckaufman@orrick.com*
VICKIE L. FEEMAN (Bar No. 177487)
Email: *vfeeman@orrick.com*
ORRICK HERRINGTON & SUTCLIFFE LLP
1000 Marsh Road
Menlo Park, CA 94025
Telephone: (650) 614-7400
Facsimile: (650) 614-7401

Attorneys for Defendants
NANYA TECHNOLOGY CORPORATION and NANYA TECHNOLOGY CORPORATION U.S.A.